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MUIRHEAD AND SATURNELLI, LLC
200 FRIBERG PARKWAY, SUITE 1001
WESTBOROUGH, MA 01581

EXAMINER	
VO, THANH DUC	
ART UNIT	**PAPER NUMBER**
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,291	CARTMELL ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on October 19, 2007. Claims 1-20 are presented for examination. Claims 1-20 are pending. All objections and rejections that are not repeated below have been withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5, 13, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5, 13, and 19 are indefinite because the relationship of "data written using the memory address", "the first memory location", "the second memory location", "a first set of commands", and "a second set of command" is unclear at to which one is "using" and which one is "used".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1, 2, 7-11, 13, 15, 16, and 18 are rejected under 35 U.S.C. 102(a) as being anticipated by Chen et al (US Patent 7,043,623).

As per claims 1, 10, and 15, Chen et al. discloses a method of accessing data memory, comprising:

a plurality of directors (Fig. 3, item 1083, where there are plurality of input and output port which require a plurality of MUX or arbiters) writing data to a first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored (See col. 8, lines 35-45);

in response to a request to read data from the memory address, reading data from the first memory location or the second memory location based on load balancing (See col. 8, lines 56-59); and

accessing data from the second memory location in response to a request to access data at the memory address when memory hardware corresponding to the first memory location has failed. See Fig. 19, and col. 8, lines 47-52, wherein the data is accessed from the backup memory when the source fails.

As per claims 2, 11, and 16, it is readily apparent to one skilled in the art that accessing the data memory includes requesting access to a specific one of the first and second memory locations is old and well known because once the data is mirrored, it can be read from either locations.

As per claims 4, 13, and 18, a method, wherein hardware coupled to the memory causes data written using the memory address to be automatically written to the first memory location and the second memory location *is an inherent feature of Chen et al. because in order for the data to be mirrored, it has to be written to two locations.*

As per claim 7, Chen et al. discloses a method further comprising:

coupling a director board to the memory (Fig. 3, item 1083); and

coupling one of: a host (Fig. 3, item 1073), a disk (Fig. 4, item 1005, wherein a computer includes a disk), and a communications link (Fig. 3, the link between the memory dispatcher to memory server) to the director board.

As per claim 8, Chen et al. discloses a method further comprising:

transferring data between the memory and the director board. See col. 7, lines 50-52.

As per claim 9, Chen et al. discloses a method further comprising:

the director board causing data to be transferred between the memory and one of: the host, the disk, and the communication link. See col. 7, lines 50 – col. 8, lines 4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 12, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Patent 7,043,623).

As per claims 3, 12, and 17, Chen et al. does not specifically disclose a method, wherein the memory address contains a portion that is common to both the first memory location and the second memory location.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the memory address of Chen et al. to include a portion that is common to both locations such as a data location index or address. The motivation of doing so is to allow the client to easily access either location by using the same data location index or address to access the data so that the client won't have to send two separate read commands in case the data in the first location is lost.

Claims 4, 14, and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Patent 7,043,623) in view of Pitts (US Patent 6,052,308).

As per claims 6, 14, and 20, Chen et al. does not disclose a method, wherein load balancing includes toggling at least one variable between a first state and a second

state and wherein data is read from the first location when the at least one variable is in the first state and from the second location when the at least one variable is in the second state.

Pitts disclosed a method of toggling in the multiplexer between the two different states so that the data accessing is balanced between the upper memory cell and the lower memory cell. It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to recognize that it is advantageous to implement the load balancing method disclosed by Pitts into the system of Lai et al. to arrive at the invention claim in claims 6 and 14. The motivation of doing so is to provide a system with more operational flexibility as well improving the speed and data sensing performance as taught by Pitts in col. 4, lines 5-10.

Following is the rejection maintain from the previous Office Action which examiner finds Applicant's argument not persuasive:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (2004/0205384) in view of Pitts (6,052,308).

As per claims 1 and 10, Lai et al. disclosed a method of accessing data memory, comprising:

writing data to a first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored (see page 2, par. 0024 and page 3, par. 0042, lines 1-10);

in response to a request to read data from the memory address, reading data from the first memory location or the second memory location (see page 3, paragraph 0042, lines 8-13); and

accessing data from the second memory location in response to a request to access data at the memory address when memory hardware corresponding to the first memory location has failed. See page 3, paragraph 0042, lines 10-13.

Lai et al. failed to teach the method of reading data from the memory locations based on load balancing. However, Pitts disclosed a method of reading the memory locations based on the load balancing (col. 5, lines 58-60). It would have been obvious to one having an ordinary skill in the art at the time of the invention to modify the system of Lai et al. to combine with the method taught by Pitts. In doing so, it would provide a system with more operational flexibility as well improving the speed and data sensing performance as taught by Pitts in col. 4, lines 5-10.

As per claims 2 and 11, Lai et al. disclosed a method, wherein accessing the data memory includes requesting access to a specific one of the first and second memory locations. See page 3, par. 0042, lines 6-8.

As per claims 3 and 12, Lai et al. disclosed a method, wherein the memory address contains a portion that is common to both the first memory location and the second memory location. See Fig. 7, item 110, wherein the address of the first and second memory modules are the same.

As per claim 4, Lai et al. disclosed a method, wherein hardware coupled to the memory causes data written using the memory address to be automatically written to the first memory location and the second memory location. See Fig. 7, item 120 and Fig. 1, item 12, wherein memory controller is hardware device.

As per claims 5 and 13, Lai et al. disclosed a method, wherein software causes data written using the memory address to be written to the first memory location and the second memory location using a first set of commands that writes the data to the first memory location and a second set of commands that writes to the second memory location. See page 3, par. 0042, lines 1-10. Furthermore, first and second set of commands are an inherent feature since a command is required in order to trigger the storage location in each of the memory module.

As per claims 6 and 14, Lai et al. failed to teach a method, wherein load balancing includes toggling at least one variable between a first state and a second state and wherein data is read from the first location when the at least one variable is in

the first state and from the second location when the at least one variable is in the second state.

Pitts disclosed a method of toggling in the multiplexer between the two different states so that the data accessing is balanced between the upper memory cell and the lower memory cell. It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to recognize that it is advantageous to implement the load balancing method disclosed by Pitts into the system of Lai et al. to arrive at the invention claim in claims 6 and 14. The motivation of doing so is to provide a system with more operational flexibility as well improving the speed and data sensing performance as taught by Pitts in col. 4, lines 5-10.

6. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (2004/0205384) in view of Pitts (6,052,308) and further in view of Hartwell et al. (2005/0160311).

As per claim 7, Lai et al. disclosed a method, further comprising:

coupling a director board to the memory (see Fig. 1, item 12); and

Lai et al. and Pitts failed to teach coupling one of: a host (mainframe), a disk, and a communications link to the director board.

Hartwell et al. taught that a host, a disk, and a communication link are connected to the memory system comprising a controller (director). See page 6, paragraph 0065, lines 4-9, and lines 11-18.

Lai, Pitts, and Hartwell are from the same field of endeavor, memory managing system.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to implement a host, disk, and communication into the system of Lai in order to arrive at the at the invention claim in claim 7. The motivation of doing so is enabling any system that requires fault tolerant memory to take the advantage of the system reliability and continuous performance as taught by Hartwell et al. in page 6, paragraph 0065 lines 1-4.

As per claim 8, Lai et al. substantially taught a method, further comprising:

transferring data between the memory and the director board. See page 2, paragraph 0027, lines 4-6.

As per claim 9, although Lai et al. and Pitts did not explicitly disclosing a director board causing data to be transferred between the memory and one of: the host, the disk, and the communication link. However, Hartwell et al. disclosed a system comprising a host (mainframe), a disk, and a communication link connected to a controller (director). Therefore, it would be readily recognized by one having an ordinary skill in the art at the time of the Applicant's invention to realize that coupling a host, disk, and communication link to the memory system comprising a memory controller inherently comprising a step of communicating among said components. The motivation of doing so is to let the host inherits the fault tolerant memory system

and therefore, the memory controller will manage the data transferring between the memory modules with the respective disk drive, host, or communicating through a communication link to broadcast or sending the requested data from clients.

7. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (2004/0205384) in view of Hartwell et al. (2005/0160311) and further in view of Pitts (6,052,308).

As per claim 15, Lai et al. disclosed a system, comprising:

an internal volatile memory (see Fig. 3, item M1); and

a plurality of directors (See Fig. 2, items 23a-23n) coupled to the memory; and

wherein each of the directors access the memory by writing data to first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored (see page 2, par. 0024 and page 3, par. 0042, lines 1-10); and

in response to a request to read data from the memory address, the directors read data from the first memory location or the second memory location (see page 3, paragraph 0042, lines 8-13); and

the directors access data from the second memory location in response to a request to access data at the memory address when memory hardware corresponding to the first memory location has failed. See page 3, paragraph 0042, lines 10-13.

Lai et al. failed to teach a plurality of disk drives. However, Hartwell et al. teaches a data storage device comprising of disk drives (see page 6, lines 11-17). It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to realize that it is advantageous to include at least one of the disk drive since the disk drive can be used to store software or firmware as taught by Hartwell et al. in page 6, lines 11-12.

Lai further failed to teach the directors are coupled to the disk drive and some of the directors are allow external access to the data storage device. However, Hartwell et al. teach a director (Fig. 1, item 108) that coupled to the disk drives said forth in the previous paragraph. It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to recognize that coupling directors to disk drives and allow the external access to the storage device is known in the computer art. In doing so, the method of data transferring is greatly improved since the director (controller) is managing the data access being executed by the central processor and communicate with the external components as taught by Hartwell in page 4, paragraph 0042, lines 1-14.

Furthermore, Lai et al. failed to teach the method of load balancing access request to the memory. However, Pitts disclosed a method of reading the memory location based on the load balancing (col. 5, lines 58-60). It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Lai et al. to combine with the method taught by Pitts. In doing so,

it would provide a system with more operational flexibility as well improving the speed and data sensing performance as taught by Pitts in col. 4, lines 5-10.

As per claim 16, Lai et al. disclosed a system, wherein the directors request access to a specific one of the first and second memory locations. See page 3, par. 0042, lines 6-8.

As per claim 17, Lai et al. disclosed a system, wherein the memory address contains a portion that is common to both the first memory location and the second memory location. See Fig. 7, item 110, wherein the address of the first and second memory modules are the same.

As per claim 18, Lai et al. disclosed a system, wherein hardware coupled to the memory causes data written using the memory address to be automatically written to the first memory location and the second memory location. See Fig. 7, item 120 and Fig. 1, item 12, wherein memory controller is hardware device.

As per claim 19, Lai et al. disclosed a system, wherein software causes data written using the memory address to be written to the first memory location and the second memory location using a first set of commands that writes the data to the first memory location and a second set of commands that writes to the second memory location. See page 3, par. 0042, lines 1-10. Furthermore, first and second set of

commands are an inherent feature since a command is required in order to trigger the storage location in each of the memory module.

As per claim 20, Lai et al. failed to teach a method, wherein load balancing includes toggling at least one variable between a first state and a second state and wherein data is read from the first location when the at least one variable is in the first state and from the second location when the at least one variable is in the second state.

Pitts disclosed a method of toggling in the multiplexer between the two different states so that the data accessing is balanced between the upper memory cell and the lower memory cell. It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to recognize that it is advantageous to implement the load balancing method disclosed by Pitts into the system of Lai et al. to arrive at the invention claim in claim 20. The motivation of doing so is to provide a system with more operational flexibility as well improving the speed and data sensing performance as taught by Pitts in col. 4, lines 5-10.

Response to Argument

8. Applicant's arguments filed October 19, 2007 have been fully considered but they are not persuasive.

With respect to Declaration under 37 C.F.R 1.131, the Remarks (pages 9-12) file on October 19, 2007 appears to repeat the same argument that Applicant previously

presented on May 04, 2007. Please refer to Office Action dated July 16, 2007 which Examiner already responded to the argument filed on May 04, 2007.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thanh D. Vo
Patent Examiner
AU 2189
01/21/2007

REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100